REMARKS

Claims 1-11 are all the claims pending in the application. By this Amendment, Applicant adds claims 5-11. Claims 5-11 are clearly supported throughout the Specification, for example, see pages 39-40 of the Specification.

In addition, in order to clarify the invention, Applicant amends claim 1. The amendment to claim 1 is made for reasons of precision of language and consistency, and does not narrow the literal scope of the claims and thus do not implicate an estoppel in the application of the doctrine of equivalents.

Preliminary Matters

Applicant thanks the Examiner for withdrawing the objections to the Specification and the claims.

Moreover, Applicant thanks the Examiner for initialing the references listed on Form PTO-1449 submitted with the Information Disclosure Statement filed on November 28, 2000. However, the Examiner failed to initial the Form PTO A& B (modified) filed with an Information Disclosure Statement on September 26, 2002. Therefore, Applicant respectfully requests that the Examiner initial the appropriate boxes on the Form PTO A& B indicating that the documents have been reviewed and return this form to the Applicant in the next office action.

Claim Rejections under 35 U.S.C. § 102

Claims 1-3 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,126,956 to Komiya et al. (hereinafter "Komiya"). Applicant respectfully traverses this

rejection and respectfully requests the Examiner to reconsider this rejection in view of the comments, which follow.

To be an "anticipation" rejection under 35 U.S.C. § 102, the reference must teach every element and recitation of the Applicant's claims. Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the reference must clearly and unequivocally disclose every element and recitation of the claimed invention.

Of these rejected claims, only claim 1 is independent. Claim 1, as now amended, among a number of unique features, recites:

> ...an available area for storing circuit elements of a circuit pattern being input;
>
> circuit pattern extracting means for making a comparison between a circuit element from the stored circuit elements of the circuit pattern being input and a corresponding circuit element...;
>
> copying means for copying the extracted circuit pattern into said available area in response to an input by an operator.

The Examiner asserts that claim 1 is directed to a ladder circuit editing system and is anticipated by Komiya. The Examiner alleges that Komiya's character generator (CG) and refresh memory (RFM) are similar to the unavailable storage means, as set forth in claim 1, that Komiya's picture memory (IMM) is similar to the available storage means, as set forth in claim 1, and that Komiya's display controller (DPC) is similar to the extracting means and copying means, as set forth in claim 1 (see pages 5-6 of the Office Action). Applicant respectfully disagrees.

Applicant has carefully studied Komiya's discussion of the method and the apparatus for displaying segments of a ladder diagram responsible for turning on an operator specified relay, which is not similar to the editing system, as set forth in claim 1. For example, if as alleged by the Examiner, the DPC and IMM of Komiya are similar to the extracting means and the available area, respectively, then the DPC does not compare a circuit element from the stored circuit elements in IMM with circuit elements of RFM and/or CG. Moreover, Komiya's IMM does not store elements from an inputted circuit, as set forth in claim 1. Finally, Komiya's copying by DPC is not in response to input by an operator.

For example, an illustrative, non-limiting embodiment of the present invention, discloses an editing system capable of autonomously retrieving analogous ladder diagrams without bothering the operator with extra work and without wasting the storage capacity of an auxiliary storage device. For example, an unavailable storage area stores at least one circuit pattern that has been previously input and the available storage area stores a new circuit pattern (the pattern being input by the operator). A circuit pattern extracting means compares a circuit element in a circuit pattern stored in the available area with a corresponding circuit element in a circuit pattern stored in the unavailable area. If the circuit elements agree, the whole circuit pattern is extracted and displayed on the input screen and the operator is asked whether this circuit pattern should be utilized. If the operator decides to utilize this circuit pattern, then the whole extracted circuit pattern is copied into the available storage. As a result, ladder diagrams are automatically retrieved. This passage is provided by way of an example only and is not intended to limit the scope of the claims in any way.

Komiya teaches a method and an apparatus for displaying a ladder diagram to facilitate debugging and maintenance by automatically searching the ladder diagram for relays involved in turning on a particular relay (col. 5, lines 46 to 51). This is done by entering the identification of the desired relay or a memory address storing the state of the relay, which in turn generates a display showing solely the segment of the ladder diagram which includes conditions for turning on a specific relay (col. 5, lines 52 to 58). Alternatively, all program segments can automatically be displayed including conditions for turning on a specific relay (col. 5, line 59 to 62).

In short, Komiya is related to automatic searching and displaying ladder diagrams for debugging purposes. Komiya is not directed to an editing and designing of ladder diagrams. As a result, Komiya fails to teach or suggest a number of features of the independent claim 1. Exemplary deficiencies of Komiya are explained in further detail below.

In particular, Komiya teaches a universal display unit 301h with a character generator CG for storing alphanumeric patterns and symbols for displaying ladder diagrams. In addition, Komiya teaches a display controller DPC, which reads each item of picture information out of the refresh memory RFM in succession and patterns corresponding to the picture information out of the character generator CG. The DPC stores the generated patterns in the picture memory IMM, which is then displayed on a display CRT. Through these operations, ladder diagram segments are displayed sequentially on the CRT in accordance with the order in which the sequence program was written (col. 8, lines 1 to 12).

The Examiner alleges that IMM and DPC correspond to the available area and extracting means, respectively, as set forth in claim 1 (see page 5 of the Office Action). However, Komiya's DPC processes data from the MEM, RFM and CG and not the IMM. The circuit patterns of IMM are simply displayed on the display CRT and are not used in any comparisons. This is consistent with Komiya's teachings of displaying a sequence program or segments of a sequence program in a ladder diagram. Once a circuit pattern(s) are generated, there is no need for further processing. The pattern(s) are simply displayed on the CRT.

In addition, it is respectfully pointed out that CG only stores alphanumeric characters and symbols in a form of a library and that DPC generates a circuit pattern using the reference guide CG and picture information of the RFM. In short, the IMM stores a DPC generated circuit pattern and not elements from an inputted circuit pattern. In fact, Komiya teaches that the operator inputs identification of the desired relay or a memory address at which the state of the desired relay is stored. Alternatively, the operator can select the item of sequence data, which indicate conditions for turning on the relay (col. 6, lines 48 to 52). This input is then used to generate a ladder diagram. The generated ladder diagram is stored in IMM for display. In short, Komiya fails to teach or suggest an available storage area for storing an inputted circuit, as set forth in claim 1.

Finally, the Examiner alleges that copying means correspond to DPC (see page 6 of the Office Action). In other words, the Examiner alleges that DPC's transferring the generated circuit patterns into IMM corresponds to both creating elements of an inputted circuit stored in the available storage area and copying the extracted circuit into the available area. However, to

extract a circuit, the elements of the inputted circuit, stored in the second available area, are used. As such, clearly the two are not identical. Moreover, the DPC generating a circuit pattern to be stored in IMM is not performed in response to an operator but rather in response to receiving a segment of a sequence program from ROM.

To sum up, extracting means, as set forth in claim 1, use the circuit elements stored in the available area for comparison, whereas in Komiya, the circuit patterns stored in the IMM are the end results of all operations by the DPC. No further operations are performed on the circuit patterns stored in the IMM, these circuit patterns are only displayed on a screen. In addition, the circuit patterns stored in the IMM are generated by the DPC and not inputted. Also, the DPC does not copy the extracted circuit pattern into the IMM based on input by an operator but rather the DPC operates based on receipt of a segment of the sequence program. At the very least, the alleged copying is not performed based on input by an operator.

In short, the DPC and the IMM of Komiya are not similar to the extracting means, the copying means and the available storage area, as set forth in claim 1. For at least these exemplary reasons, Applicant respectfully submits that independent claim 1 is patentably distinguishable from Komiya. Applicant therefore respectfully requests the Examiner to reconsider and withdraw this rejection of independent claim 1. Also, Applicant respectfully submits that claims 2-3 are allowable at least by virtue of their dependency on claim 1.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claim 4 contains allowable subject matter. However, Applicant does not acquiesce to any inferences or presumptions drawn from the Examiner's statement regarding the reasons for allowance. Moreover, Applicant respectfully holds the rewriting of claim 4 in abeyance until the arguments presented with respect to independent 1 have been reconsidered.

New claims

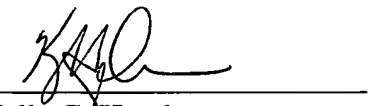
In order to provide more varied protection, Applicant adds claims 5-11. Claim 5 is patentable over Komiya at least by virtue of its recitation of *circuit pattern extracting means for making a comparison between a circuit element of the circuit pattern stored in the available storage area and a corresponding circuit element.* Claims 6-10 are patentable at least by virtue of their dependency on claim 5. In addition, claim 11 is clearly patentable over the reference cited by Examiner, at least by virtue of reciting *selecting said each displayed circuit pattern by an operator.*

Conclusion and request for a telephone interview.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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